How to Keep a FLYBACK Switch Mode Supply Stable with a Critical-Mode Controller

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APPLICATION NOTE

INTRODUCTION

Switch Mode Power Supplies (SMPS) can operate in two different conduction modes, each one depicting the level of the current circulating in the power choke when the power switch is turned on. As will be shown, the properties of two black boxes delivering the same power levels but working in different conduction modes, will change dramatically in DC and AC conditions. The stress upon the power elements they are made of will also be affected. This article explains why the vast majority of low-power FLYBACK SMPS (off-line cellular battery chargers, VCRs, etc.) operate in the discontinuous area and present a new integrated solution especially dedicated to these particular converters.

Defining the Mode

Figures 1. (a) and 1. (b) show the general shape of a current flowing through the converter's coil during a few cycles. In the picture, the current ramps up when the switch is closed (ON time) building magnetic field in the inductor's core. When the switch opens (OFF time), the magnetic field collapses and, according to LENZ's law, the voltage across the inductance reverses. In that case, the current has to find some way to continue its flow and start its decrease (in the output network for a FLYBACK, through the freewheel diode in a BUCK etc.).

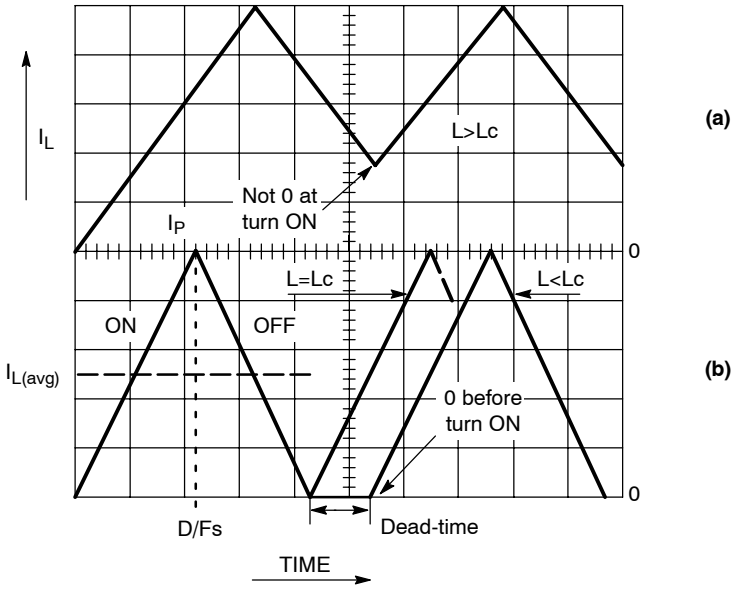


Figure 1.

If the switch is switched ON again during the ramp down cycle, before the current reaches zero (Figure 1.), we talk about Continuous Conduction Mode (CCM). Now, if the energy storage capability of the coil is such that its current dries out to zero during OFF time, the supply is said to operate in Discontinuous Conduction Mode (DCM). The amount of dead-time where the current stays at a null level defines how strongly the supply operates in DCM. If the

September, 2000 – Rev. 0
Publication Order Number:
AN1681/D

current through the coil reaches zero and the switch turns ON immediately (no dead-time), the converter operates in Critical Conduction Mode.

Where is the Boundary?

There are three ways you can think of the boundary between the modes. One is about the critical value of the inductance, L_C, for which the supply will work in either CCM or DCM given a fixed nominal load. The second deals with a known inductance L. What level of load, R_C, will push my supply into CCM? Or what minimum load my SMPS should see before entering DCM? The third one uses fixed values of the above elements but adjusts the operating frequency, F_C, to stay in critical conduction. These questions can be answered after a few lines of algebra corresponding to Figure 2. 's example, a FLYBACK converter:

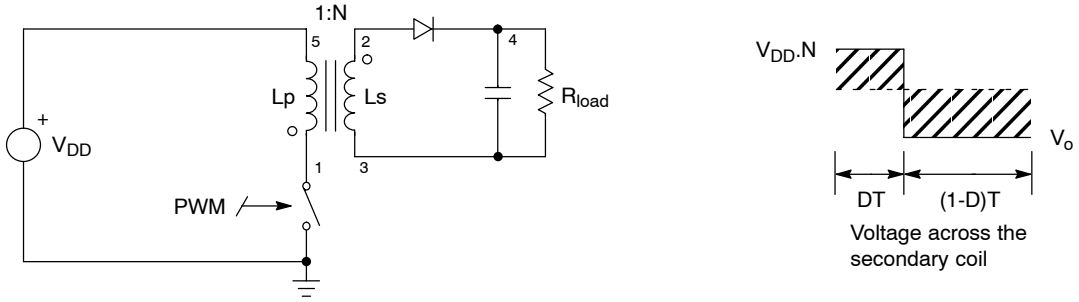


Figure 2.

To help determine some key characteristics of this converter, we will refer to the following statements:

- The average inductor voltage per cycle should be null (1)
- From Figure 1. (b), when $L=L_C$, $I_{L(avg)} = Ip/2$ (2)
- A 100% efficiency leads to $P_{in}=P_{out}$ (3)

The DC voltage transfer ratio in CCM is first determined using statement (1), thus equating Figure 2. (b)'s areas:

$$V_{DD} \cdot N \cdot D = V_o \cdot (1 - D).$$

After factorization, it comes

$$\frac{V_{out}}{V_{in}} = \frac{D}{(1 - D)} \cdot N \text{ (4)}.$$

As we can see from Figure 1. (b), the flux stored in the coil during the ON time is down to zero right at the beginning of the next cycle when the inductance equals its critical value ($L=L_C$). Mathematically this can be expressed by integrating the formula:

- $V_L \cdot dt = L \cdot dI_L$ thus, $\int_0^{\frac{D}{Fs}} V_L \cdot dt = L_c \cdot \int_0^{Ip} dI_L$.

  $\Rightarrow \frac{V_{in} \cdot D}{Fs} = L_C \cdot Ip = 2 \cdot I_{L(avg)} \cdot L_C$, from (2).
- From (3), $V_{in} \cdot I_{L(avg)} = I_o \cdot (V_{in} \cdot N + V_{out})$, or

  $I_{L(avg)} = I_o \cdot (N + \frac{V_{out}}{V_{in}})$
- By definition, $I_o = \frac{V_{out}}{R}$ and $V_{out} = V_{in} \cdot N \cdot \frac{D}{1 - D}$ from (4).

If we introduce these elements in the above equations, we can solve for the critical values of R_C, L_C and F_C:

$$R_C = \frac{2 \cdot L_C \cdot Fs \cdot N^2}{(1 - D)^2}$$

$$L_C = \frac{R_C \cdot (1 - D)^2}{2 \cdot Fs \cdot N^2}$$

$$F_C = \frac{R_C \cdot (1 - D)^2}{2 \cdot L_C \cdot N^2}$$

Filling-in the Bucket

The FLYBACK converter, as with the BOOST and BUCK-BOOST structures, has an operating mode comparable to someone filling a bucket (coil) with water and flushing it into a water tank (capacitor). The bucket is first presented to the spring (ON time) until its inner level reaches a defined limit. Then the bucket is removed from the spring (OFF time) and flushed into a water tank that supplies a fire engine (load). The bucket can be totally emptied before refilling (DCM) or some water can remain before the user presents it back to the spring (CCM). Let's suppose that the man is experimented and he ensures that the recurrence period (ON+OFF time) is constant. The end-user is a fireman who closes the feedback loop via his voice, shouting for more or less flow for the tank. Now, if the flames suddenly get bigger, the fireman will require more power from its engine and will ask the bucket man to provide the tank with a higher flow. In other words, the bucket operator will fill his container longer (ON time

increases). BUT, since by experience he keeps his working period constant, the time he will spend in flushing into the tank will naturally diminish (OFF time decreases), so will the amount of water poured. The fire engine will run out of power, making the fireman shout louder for more water, extending the filling time etc. The loop oscillates! This behavior is typical for converters in which the energy transfer is not direct (unlike the BUCK derived families) and severely affects the overall dynamic performances. In time domain, a large step load increase requires a corresponding percentage rise of the inductor current. This necessitates a temporary duty-cycle augmentation which (with only two operational states) causes the diode conduction time to diminish. Therefore, it implies a decrease in the average diode current at first, rather than an increase as desired. When heavily into the continuous mode and if the inductor current rate is small compared to the current level, it can take many cycles for the inductor current to reach the new value. During this time, the output current is actually reduced because the diode conduction time (TOFF) has been decreased, even if the peak diode current is rising. In DCM, by definition, a third state is present whether neither the diode or the switch conduct and the inductor current is null. This « idle time» allows the switch duty cycle to lengthen in presence of a step load increase without lowering the diode conduction time. In fact, it is possible for the DCM circuit to adapt perfectly to a step load change of any magnitude in the very first switching period, with the switch conduction time, the peak current, and the diode conduction time all increasing at once to the values that will be maintained forevermore at the new load current.

The extra delay is mathematically described by a Right Half-Plane Zero (RHPZ) in the transfer function

$$(Av = \frac{(1 - S_z1) \cdot ...}{...})$$

and forces the designer to roll-off the loop gain at a point where the phase margin is still secure. Actually, a classical zero in the Left Half-Plane

$$(Av = \frac{(1 + S_z1) \cdot ...}{...})$$

provides a boost in gain AND phase at the point it is inserted. Unfortunately, the RHPZ gives a boost in gain, but lags the phase. More viciously, its position moves as a function of the load which makes its compensation an almost impossible exercise. Rolling-off the gain well under the worse RHPZ position is the usual solution. Let's also point out that the low-frequency RHPZ is only present in FLYBACK type converters (BOOST, BUCK-BOOST) operating in CCM and moves to higher-frequencies (then becoming negligible) when the power supply enters DCM. The loop compensation becomes easier. For additional information, reference [1] gives an interesting *experimental* solution to cure the BOOST from its low-frequency RHPZ.

How Can I Model My Converter?

Two main solutions exist to carry AC and DC studies upon a converter. The first one is the well known State-Space Averaging (SSA) method introduced by R. D. MIDDLEBROOK and S. CÙK in 1976 [2] that leads to average models. In the modeling process, a set of equations describes the electrical characteristics of a switching system for the two stable positions of the switches, as Figures 3. (a) and 3. (b) portrait for a BOOST type converter.

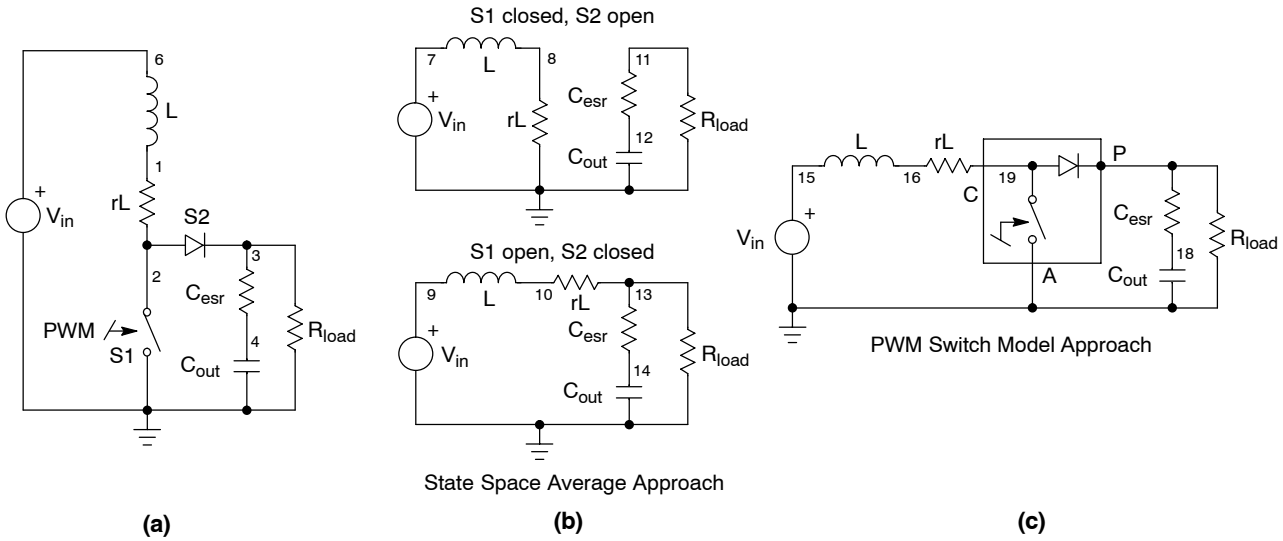


Figure 3.

The SSA technique consists in smoothing the discontinuity associated with the transition between these two states, then deriving a model where the switching component has disappeared in favor of a unique state equation describing the average behavior of the converter. The result is a set of continuous nonlinear equations in which the state coefficients now depend upon the duty cycles **D** and **D'** (1-D). A linearization process will finally lead to a set of continuous linear equations. The reader interested by an in-depth and pedagogical description of these methods will find all the necessary information in Daniel MITCHELL's book [3].

As one can see from Figure 3. , the SSA models the converter in its entire electrical form. In other words, the process should be carried over all the elements of the converter, including various in/out passive components. Depending on the converter structure, the process can be very long and complicated.

In 1988, Vatché VORPERIAN, from Virginia Polytechnic Institute (VPEC), developed the concept of the Pulse Width Modulation (PWM) switch model [4]. VORPERIAN considered simply modeling the power switch alone, and then inserting an equivalent model into the converter schematic, in exactly the same way as it is done when studying the transfer function of a bipolar amplifier (Figure 3. (c)). With his method, VORPERIAN demonstrated among other results, that the flyback converter operating in DCM was still a second order system, affected by high-frequency second pole and RHPZ. An introduction to simulating with VORPERIAN's models is detailed in reference [5].

The Bode Plot of the FLYBACK Converter

From the previous works, the poles and zeroes of converters operating in DCM and CCM have been extracted, giving the designer the necessary insight to make a power supply stable and reliable. The following summary gives their positions in function of the operating mode, and also specifies the various gain definitions for a FLYBACK converter:

	DCM	CCM
1st order pole	$\frac{2}{2 \cdot \pi \cdot R_{load} \cdot C_{out}}$	
2nd order pole	High frequency pole, see reference [4]	$\frac{(1 - D)}{2 \cdot \pi \cdot \sqrt{L_{sec} \cdot C_{out}}}$
Left Half-Plane Zero	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$	$\frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}}$
Right Half-Plane Zero	High frequency RHPZ, see reference [4]	$\frac{R_{load} \cdot (1 - D)^2}{2 \cdot \pi \cdot L_{sec} \cdot D}$
V_{output}/V_{input} DC Gain	$N \cdot D \cdot \sqrt{\frac{R_{load}}{2 \cdot L_P \cdot F_{SW}}}$	$\frac{D}{(1 - D)} \cdot N$
V_{output}/V_{error} DC Gain	$\frac{V_{input}}{V_{SAW}} \cdot \sqrt{\frac{R_{load}}{2 \cdot L_P \cdot F_{SW}}}$	$\frac{V_{input}}{V_{SAW}} \cdot \left(1 + \frac{V_{output}}{V_{input}}\right)^2$

F_{SW} = switching frequency
V_{SAW} = sawtooth amplitude of the oscillator's ramp
L_P = primary inductance
L_{sec} = secondary inductance

The Bode plots can be generated in a multitude of manual methods or in a more automated way by using a powerful dedicated software such as POWER 4−5−6 [6]. We have asked the program to design two 100 kHz voltage-mode SMPS with equivalent output power levels, but operating in different modes. The results are given below (Figure 4.), including the high-frequencies pole and RHPZ in DCM, as described in [4].

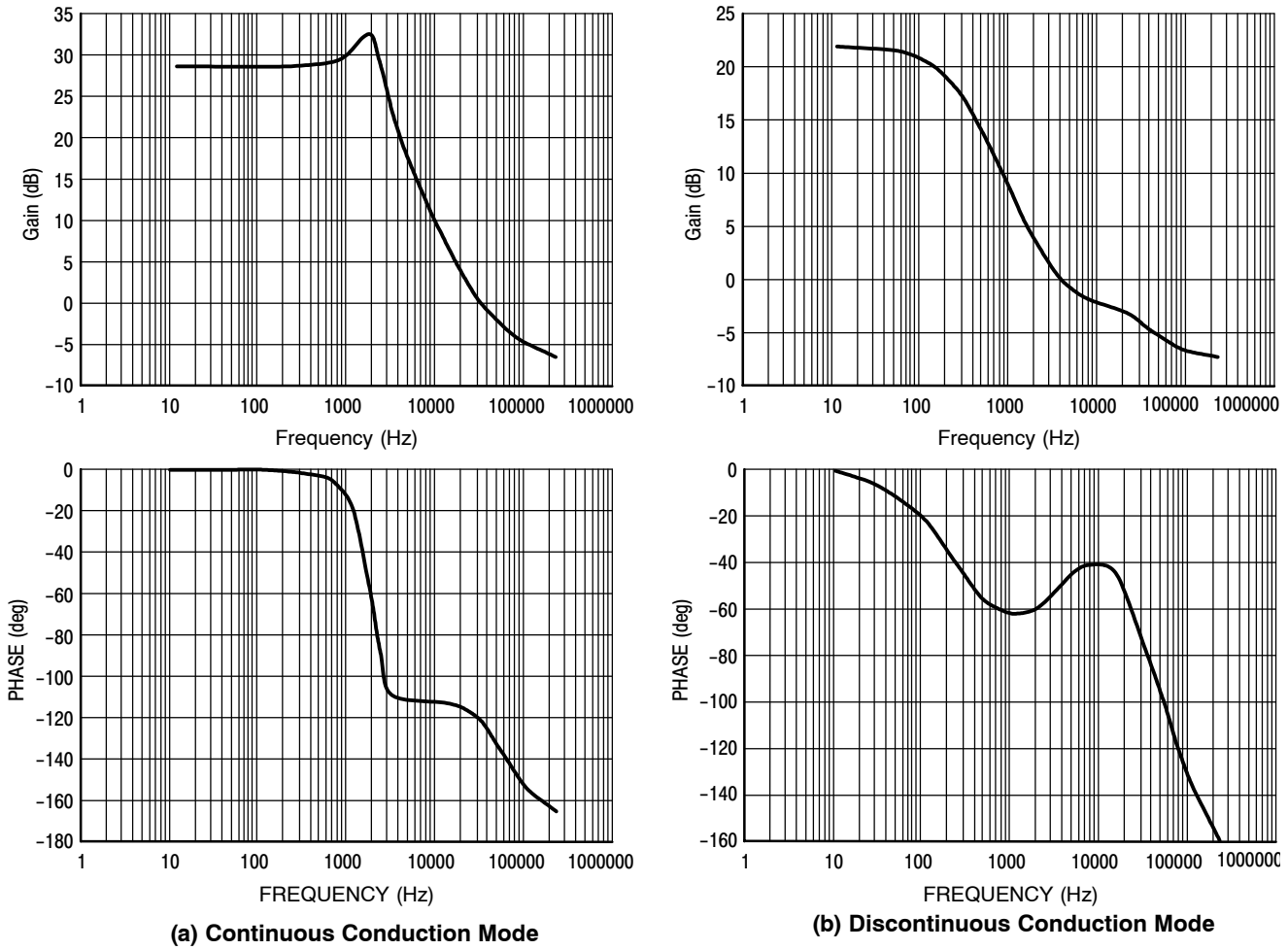


Figure 4.

From the above pictures, it is clear that the DCM converter will require a simple double-pole single zero compensation network (type 2 amplifier), while a two-pole two-zero type 3 amplifier appears to be mandatory to stabilize the CCM converter. Furthermore, the CCM's second order pole moves in relationship to the duty cycle while the poles/zeroes are fixed in DCM.

SPICE Simulations of the Converter

One can distinguish between two big families of converter SPICE models, average and switching. The average models implement either the SSA technique or the VORPERIAN's solution. Since no switching component is associated with these models, they require a short computational time and can work in AC or TRANSIENT analysis. Some support large transient sweeps, while some only accept small-signal conditions. On the other side, switching models are the SPICE reproduction of the breadboard world and simulate the supply using the PWM controller you selected or the MOSFET model given by its manufacturer. Both models have their own advantages: average models simulate fast, but by definition, they cannot include leakage energy spikes or parasitic noise effects. Switching models take longer time to run because the simulator has to perform a thin analysis (internal step reduction) during each commutation cycles but since parasitic elements can be included, they allow the designer to dive into the nitty-gritty of the converter under study. Reference [7] will guide you in case you would like to write a switching model yourself.

SPICE models are available from several sources, but INTUSOFT (San Pedro, CA), the IsSpice4 editor, has recently released his new SMPS library which gathers numerous average and switching models. Among these models, we will describe a very simple and accurate model which has been developed by Sam-BEN-YAAKOV from Ben-Gurion university (ISAREL). This model converges well and finds its DC point alone. Finally, it allows AC simulations as well as large signal sweeps. The netlist is given below:

```
**** Sam BEN-YAAKOV FLYBACK's Model ****
.SUBCKT FLYBACK DON IN OUT GND {FS=??? L=??? N=???}
BGIN IN GND I=I(VLM)*V(DON)/(V(DON)+V(DOFF))
BELM OUT1 GND V=V(IN)*V(DON)-V(OUT)*V(DOFF)/{N}
RM OUT1 5 1M
LM 5 8 {L}
VLM 8 GND
BGOUT GND OUT I=I(VLM)*V(DOFF)/{N}/(V(DON)+V(DOFF))
VCLP VC 0 9M
D2 VC DOFF DBREAK
D1 DOFF 6 DBREAK
R4 DOFF 7 10
BDOFFM 6 GND V=1−V(DON)−9M
BDOFF 7 GND V=2*I(VLM)*{FS}*{L}/V(DON)/V(IN)−V(DON)
.MODEL DBREAK D (TT=1N CJO=10P N=0.01)
.ENDS
```

The implementation of the model is really straightforward, as demonstrated by Figure 5. schematic which shows the converter we already dimensioned with the help of POWER 4−5−6.

(a)

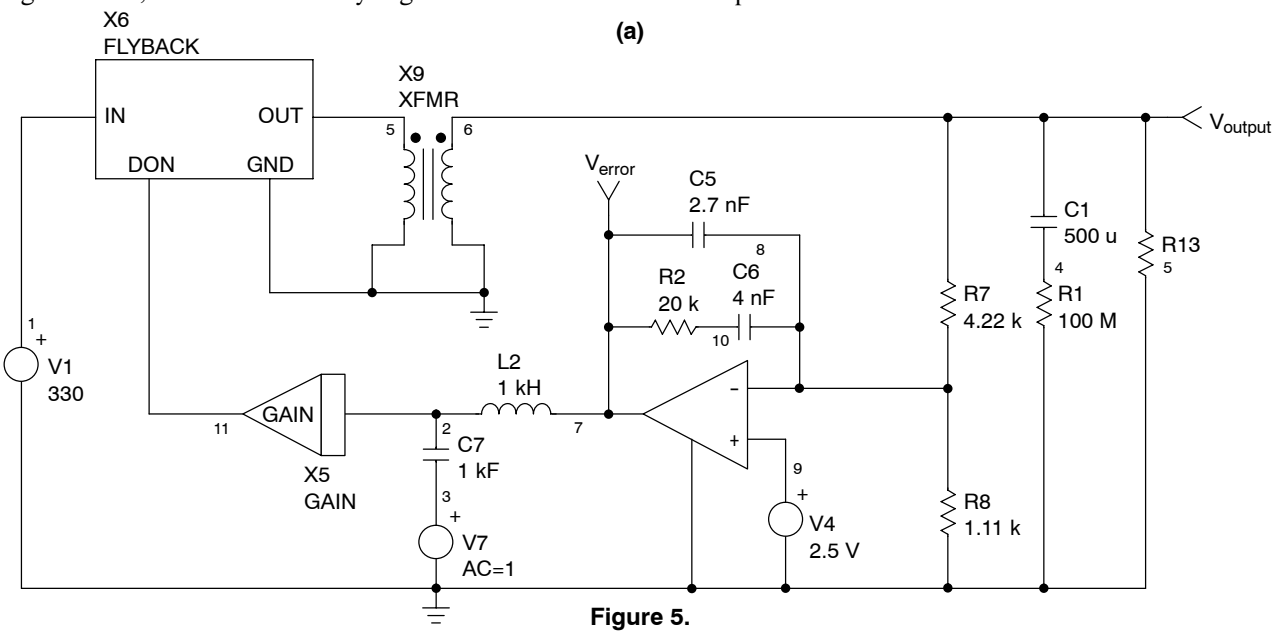


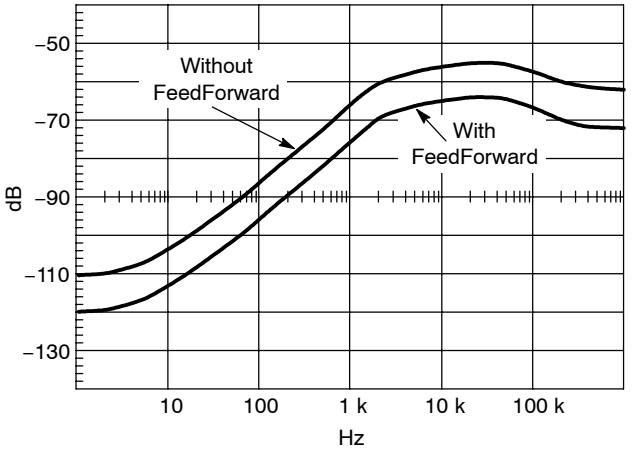
Figure 5.

It is interesting to temporarily open the loop and conduct AC simulations in order to isolate the error amplifier in AC and let you adjust the compensation network until the specifications are met. The fastest way to open the loop is to include an LC network as depicted in the above schematic (L2−C7). The inductive element maintains the DC error level such that the output stays at the required value. But it stops any AC error signal that would close the loop. The C element gives an AC signal injection thus allowing a normal AC sweep. To do so, let L2 1 kH and C7 1 kF. In the opposite sense, run a TRANSIENT by decreasing L2 to 1 nH and C7 to 1 pF. This method presents the advantage of an automatic DC duty cycle adjustment and allows you to quickly modify the output parameter without tweaking the duty source at every change.

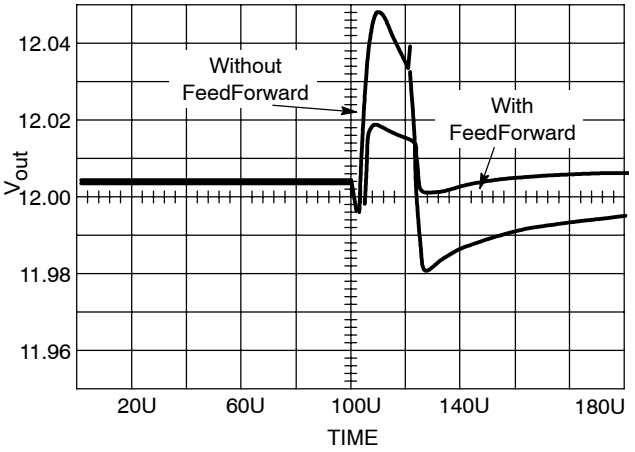
The error amplifier model is directly derived from the specifications given by the controller's data-sheets you selected. A simplified macro-model can be built and simulated as reference [7] details. You can also directly include a full detailed component to highlight the impact of its key parameters upon the supply under study (slewrate etc.). X5 subcircuit simulates the gain introduced by the PWM modulator. You can see it as a box converting a DC voltage (the error amplifier voltage) into a duty cycle D. The average models accept up to 1 volt as a duty cycle control voltage (D=100%). Generally, the IC's oscillator sawtooth can swing up to 3 or 4 volts, thus forcing the internal PWM stage to deliver the maximum duty cycle when the error amplifier reaches this value. To account for the 1 volt maximum input of our average models, the insertion of an attenuator with 1/VSAW ratio after the error amplifier output is mandatory. For example, if the sawtooth amplitude of the integrated circuit we use is 2.5 VPP, then the ratio will be: 1/2.5=0.4.

These kinds of SPICE circuits let you immediately check the parameters of interest without sacrificing your time in

watching the machine computing! The audio susceptibility is delivered in a snap shot, as Figure 5. (b) portraits. Adding a bit of feedforward with a simple source in series with X5's output (500U*V(1)) gives you, as expected, a better behavior. The transient response to an input step does not take longer, as Figure 5. (c) depicts (10 V input step) for both of the previous conditions.



(b)



(c)

Figure 5. (Continued)

A Critical Mode Controller

As we saw, keeping your SMPS in the discontinuous mode will let you to design the compensation network in a more easy way. It will also ensure a stable and reliable behavior as long as you stay in the discontinuous area. How can you be sure to stay in DCM, regardless the load span you apply at the output?? Two solutions: a) you calculate L_P in order to always stay in DCM, but you assume to know all load conditions. b) you permanently adjust the switching frequency to stay DCM, whatever the load is. This last solution has been adopted in the MC33364 from ON Semiconductor (Phoenix, AZ). The critical conduction controller ensures a switch turn on immediately after the primary current has dropped to zero. In this case, you do no longer worry about the values your load will take since the controller tunes its frequency to keep the SMPS in DCM. The stability is then guaranteed over the full load range.

Am I Critical?

To answer this question, the controller needs to know the level of the primary current. The most economical solution exploits the signal delivered by the auxiliary winding. When this one has fallen to zero, an internal set is delivered to the latch, initiating a new cycle. In case the synchronization signal would be lost, or when using the IC in a standalone application, an internal watchdog timer restarts the converter if the driver's output stays off more than 400 μs after the inductor current has reached zero.

Output Switching Frequency Clamp

As we already said, the system adjusts its frequency to maintain the DCM. However, in absence of load, the operational frequency can shift to high values, engendering unacceptable switching losses and making the design of the EMI filter a difficult task. To circumvent this intrinsic problem, the designers of the IC have added an internal frequency clamp whose function is to limit the maximum excursion. The MC33364 is thus declined in two versions including or not the clamping capability: 33364D and D1 limit to 126 kHz the upper value of the switching frequency, while the 33364D2 does not host this feature.

Good Riddance Startup Resistor!

The majority of offline SMPS are self supplied. A startup resistor charges a bulk capacitor until the IC's undervoltage limit is reached. While the bulk capacitor voltage begins to decrease, the circuit starts to actuate the switching transistor and the auxiliary supply feeds the controller back through the rectifier. But once the steady-state level is reached, the startup resistor is still there and wastes some substantial energy in heat. In low power SMPS, you hunt down any source of wasted power to raise the overall efficiency at an acceptable value. Figure 6. shows the method ON Semiconductor has implemented in the 33364 to quash the startup element.

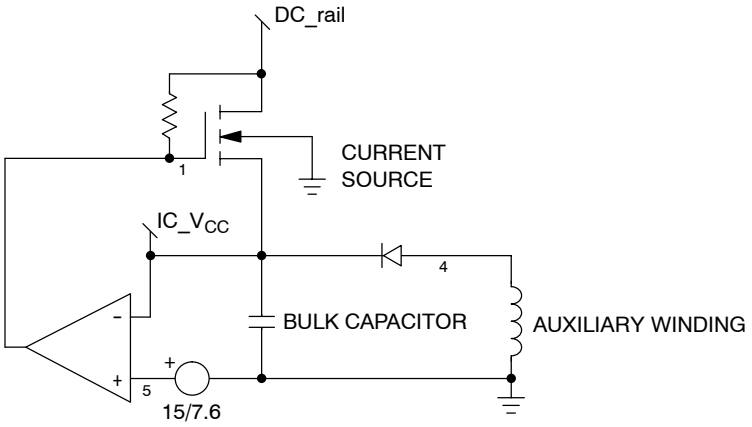


Figure 6.

It works as follow: when the mains is first applied to the converter, the MOSFET charges up the bulk capacitor until the voltage on its pins reaches the startup threshold of 15 V. At this time, the MOSFET opens and the circuit operates by itself.

A Low Part-count Converter

The 33364 has been specifically designed to save a maximum of parts. Figure 7. illustrates this will for an economical 12 W AC/DC wall adapter.

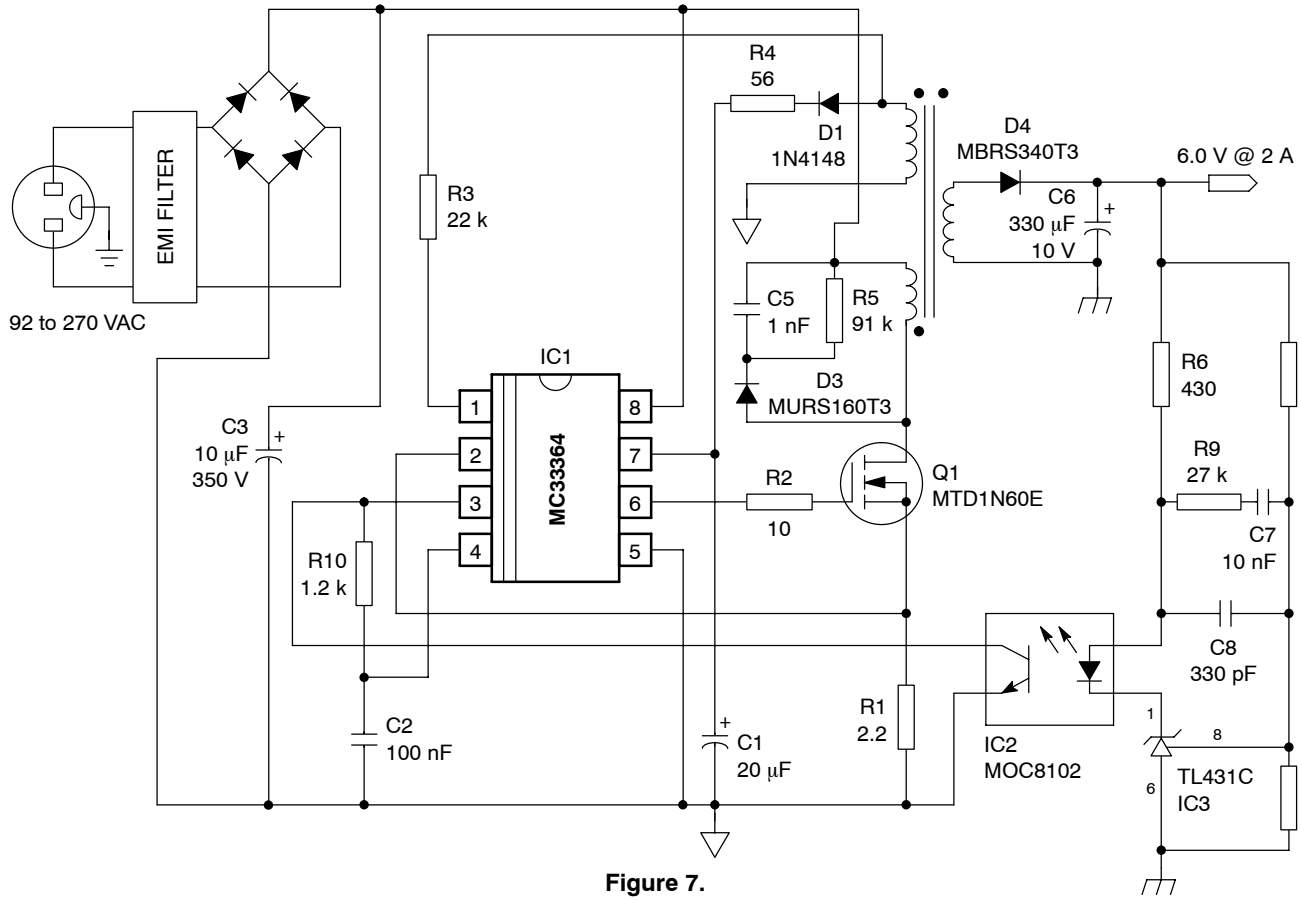


Figure 7.

The leakage energy spike is clipped by the R5−C5 network whose second function is to smooth the rising drain voltage, correspondingly limiting the radiated noise. This last feature is unfortunately no longer valid when you use a clipping circuit made of a fast rectifier and a zener diode. The circuit's sensitivity to the noise present on the sense resistor is largely diminished by the implementation of a leading edge blanking network. This system blanks the starting portion of the primary ramp-up current which can

be the seat of spurious spikes: a resonance with the parasitic inter-winding capacitors and the ON gate-source current.

Since every current mode converter are inherently unstable over a certain duty-cycle value, it can be wise to add some current ramp compensation even in DCM, as Ray RIDLEY demonstrated in the 90's [8]. How can you provide the 33364 sense input with some ramp to since no oscillator pinout is available? Figure 8. shows a possible solution by integrating the driver's output. The resulting linear ramp will add to the sense information, thus stabilizing the converter. You can also adopt this method in other cases, even when the oscillator's ramp is available. The integrator solution prevents the internal oscillator to be externally loaded which in certain circumstances can lead to erratic behaviors.

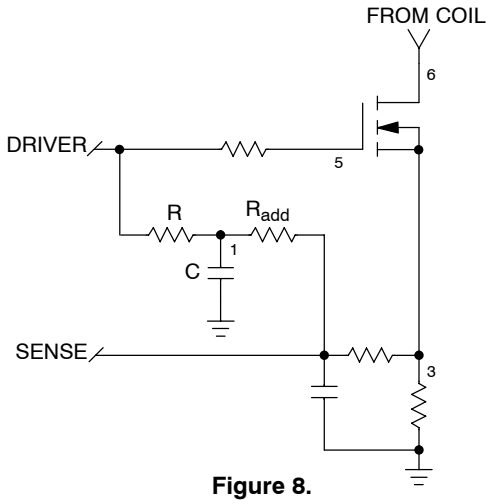


Figure 8.

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Notes

Notes

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